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Application / Conf. No.	10/086,129 / 2232
Filing Date	February 28, 2002
First Named Inventor	David P. Schultz
Examiner Name	Unassigned
Group Art Unit	2133
Issue Fee Batch No.	
Attorney Docket Number	X-1069 US

ENCLOSURES (check all that apply)

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| <input type="checkbox"/> Fee Transmittal Form | <input type="checkbox"/> Assignment Papers
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1.52 or 1.53 | | |

Remarks

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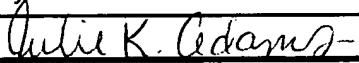
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IN THE UNITED STATES PATENT OFFICE

Applicants: David P. Schultz
Assignee: Xilinx, Inc.
Title: METHOD AND SYSTEM FOR FLEXIBLY NESTING JTAG TAP
CONTROLLERS FOR FPGA-BASED SYSTEM-ON-CHIP (SoC)
Serial No.: 10/086,129 File Date: 2-28-02
Examiner: Unassigned Art Unit: 2133
Docket No.: X-1069 US

COMMISSIONER FOR PATENTS
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INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant brings to the attention of the Examiner the twelve (12) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

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Respectfully submitted,

MAY 02 2002

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H. C. Chan
Attorney for Applicant
Reg. No. 35,477
408-879-6149

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Julie K. Adams
Name

Julie K. Adams
Signature

HCC: jka